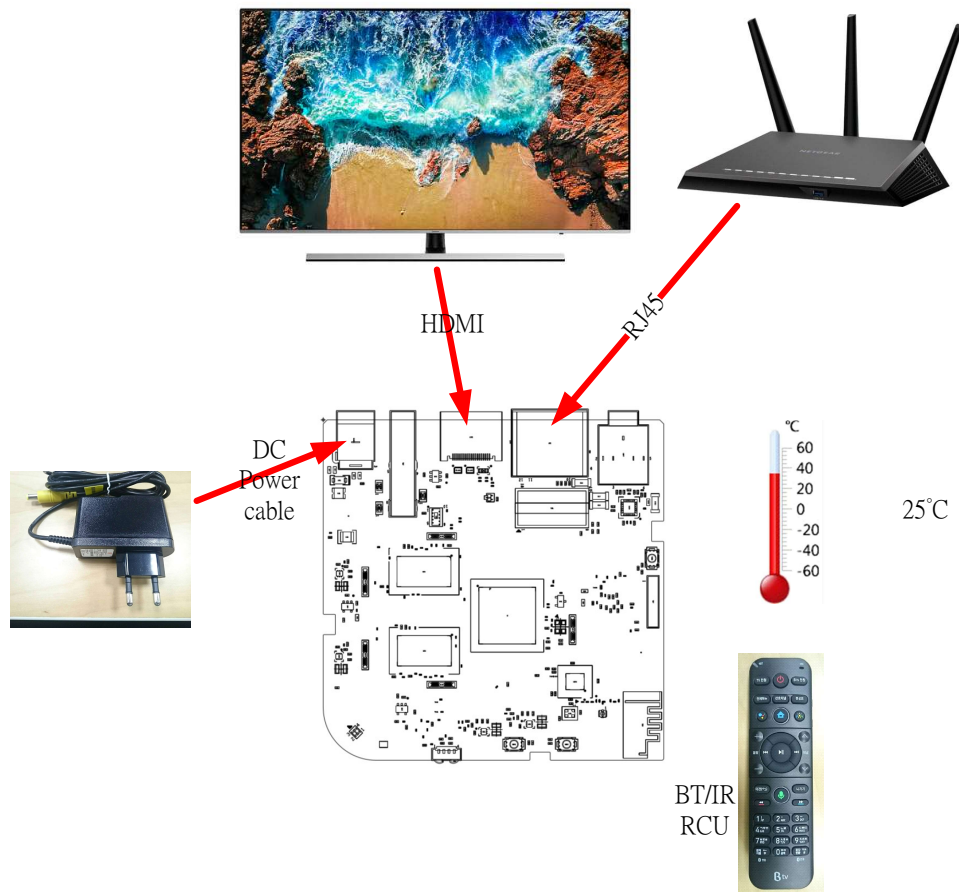


Hardware Unit Test Report

Power Accuracy Test

Hardware version	FW version	Sample No.	eMMC Flash P/N
V005	4.9.113 #1 Mon Feb 11 22:40:43 CST 2019	S/N:	KLM8G1GETF-B041

1. Power Test Setup (1)



1.1 Test Condition

BOX play 4K video via Ethernet by using YouTube. HDMI output port connects to TV through HDMI cable. The temperature is about 25 degrees.

1.2 Result and Picture

Power Rail	Specification (V) (+5%)			Test Result (V)	Figure	Pass/Fail
	Min.	Typ.	Max.			
PP_PWR_IN (5V)	4.75	5	5.25	5.068	Figure 1	Pass
HDMI_PW (5V)	4.75	5	5.25	5.093	Figure 2	Pass
USB_5V (5V)	4.75	5	5.25	5.109	Figure 3	Pass
VDD_EE(0.8V)	0.77	0.8	0.9	0.846	Figure 4	Pass
VDDCPU *	0.68	1	1.03	1.012	Figure 5	Pass
P3V3 (3.3V)	3.15	3.3	3.45	3.364	Figure 6	Pass
P2V5 (2.5V)	2.375	2.5	2.625	2.516	Figure 7	Pass
P1V8 (1.8V)	1.71	1.8	1.89	1.814	Figure 8	Pass
EMMC_VDDQ (1.8V)	1.71	1.8	1.89	1.818	Figure 9	Pass
P1V2 (1.2V)	1.14	1.2	1.26	1.203	Figure 10	Pass

Note * VDDCPU power rail is using voltage identification and control by PWM. This report is fix in 1V.

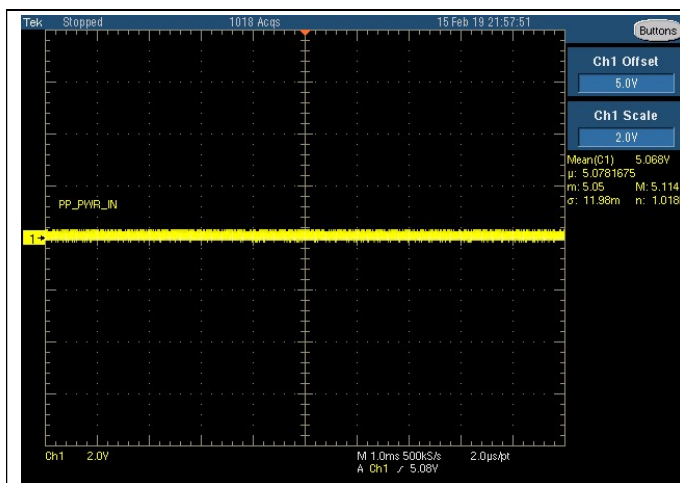


Fig. 1: PP_PWR_IN



Fig. 2: HDMI_PW

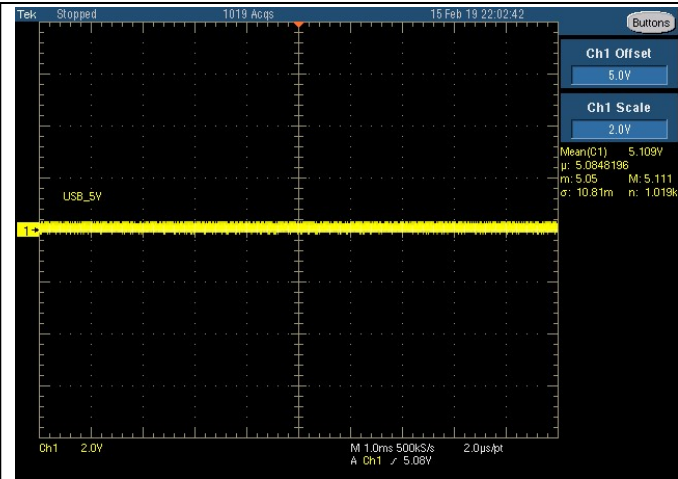


Fig. 3: USB_5V

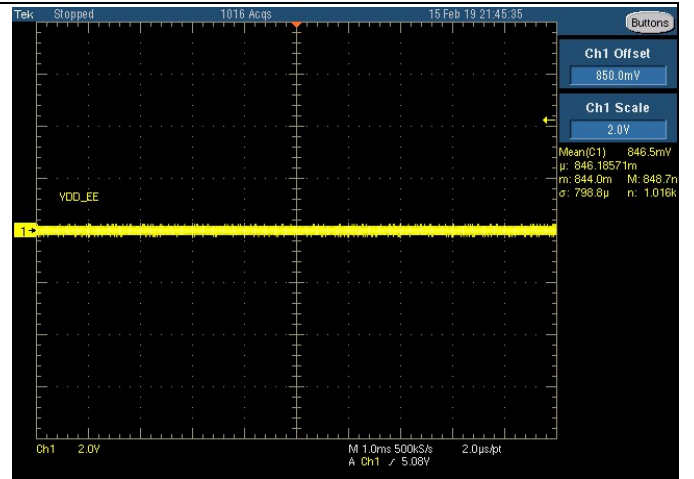


Fig. 4: VDD_EE

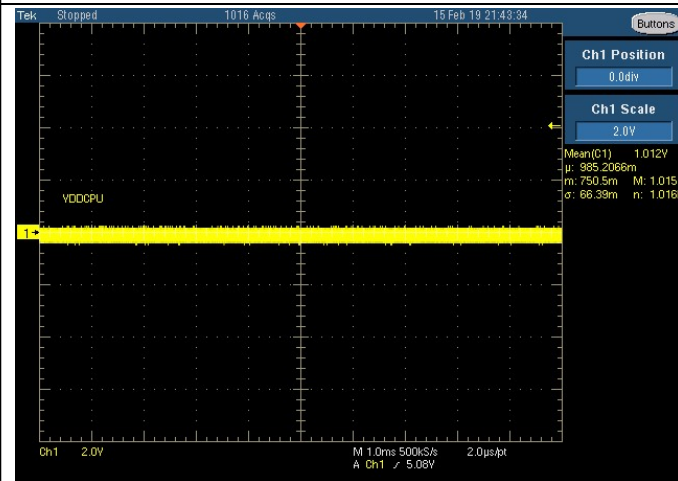


Fig. 5: VDDCPU

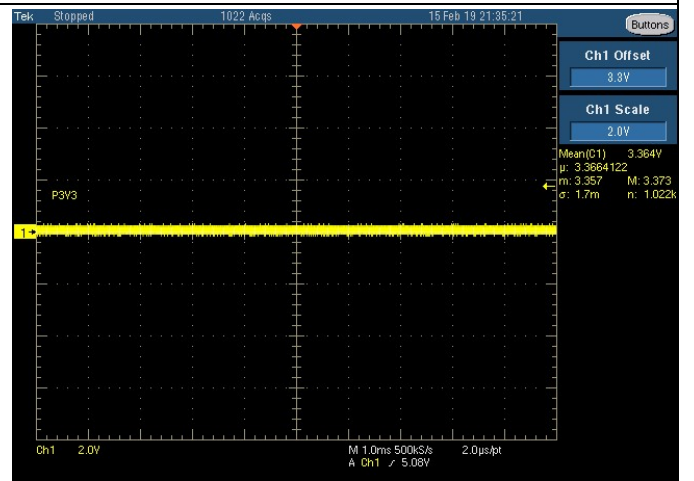


Fig. 6: P3V3

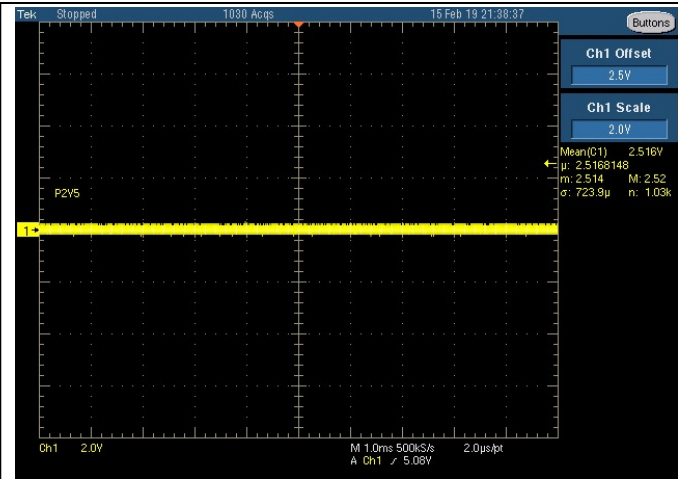


Fig. 7: P2V5

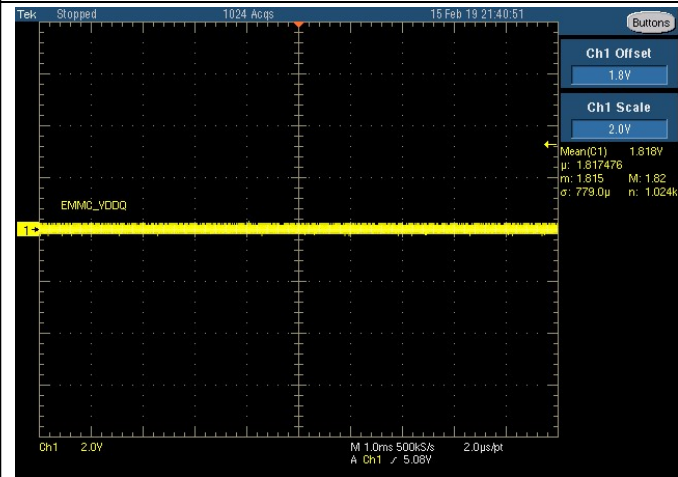


Fig. 9: EMMC_VDDQ

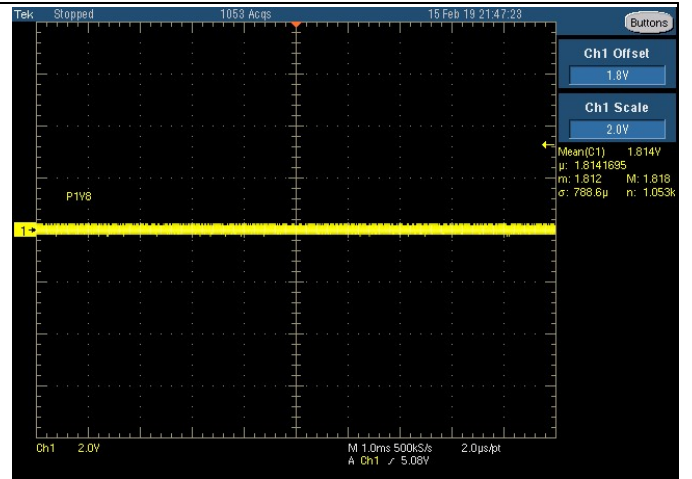


Fig. 8: P1V8

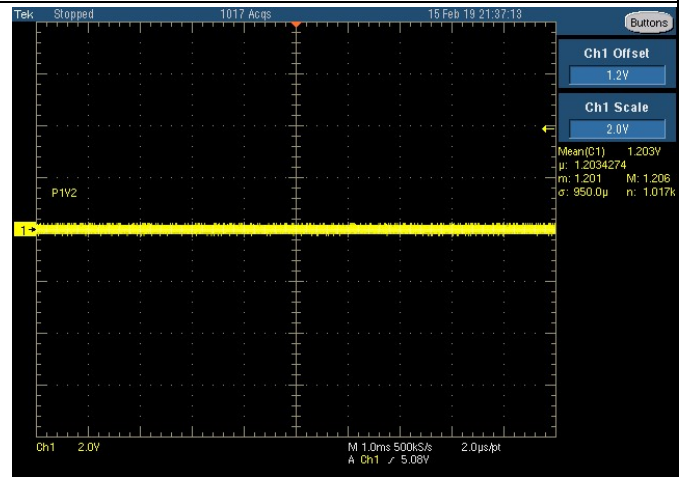
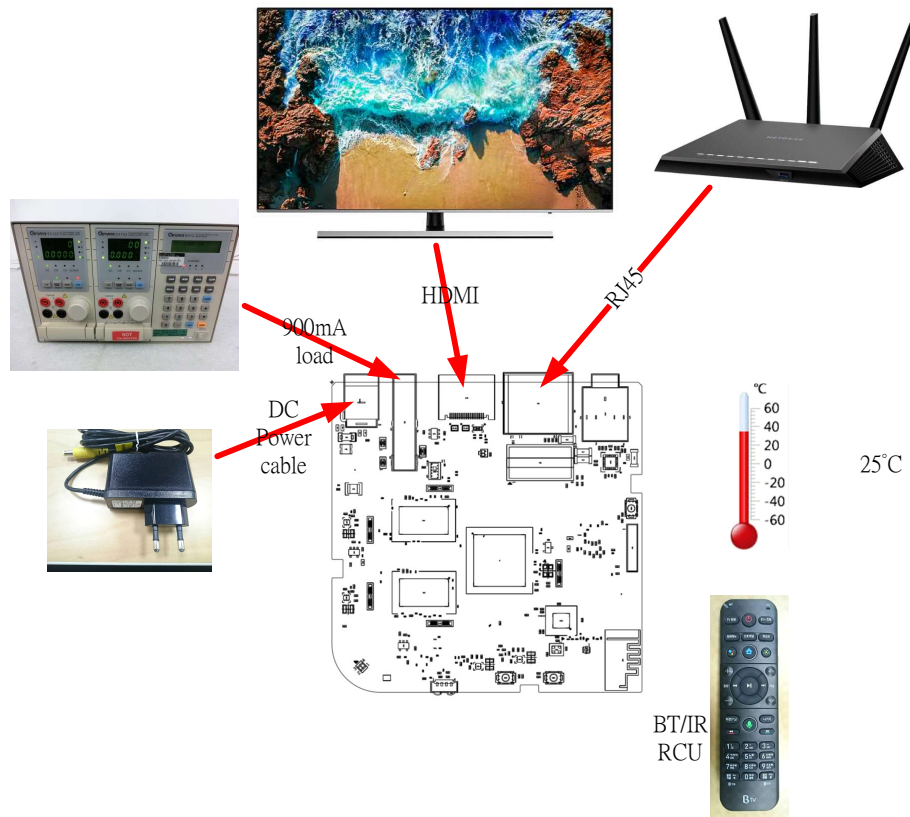


Fig. 10: P1V2

2. Power Test Setup (2)



2.1 Test Condition

BOX play 4K video via Ethernet by using YouTube. The USB port is loading with 900mA. HDMI output port connects to TV through HDMI cable. The temperature is about 25 degrees.

2.2 Result and Picture

Power Rail	Specification (V) (+/-5%)			Test Result (V)	Figure	Pass/Fail
	Min.	Typ.	Max.			
PP_PWR_IN (5V)	4.75	5	5.25	4.936	Figure 11	Pass

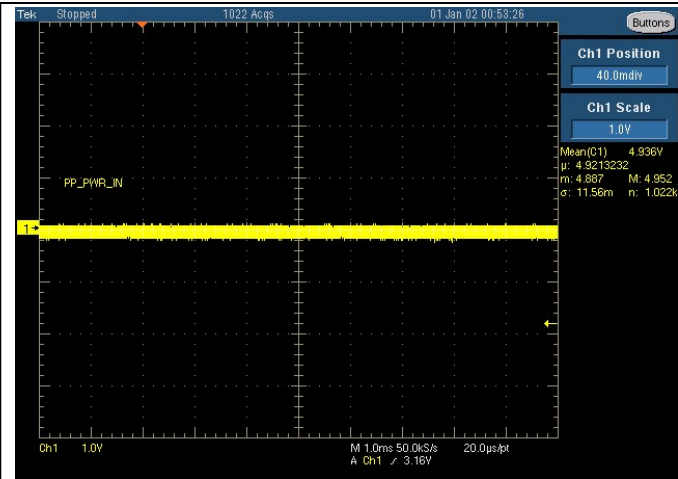
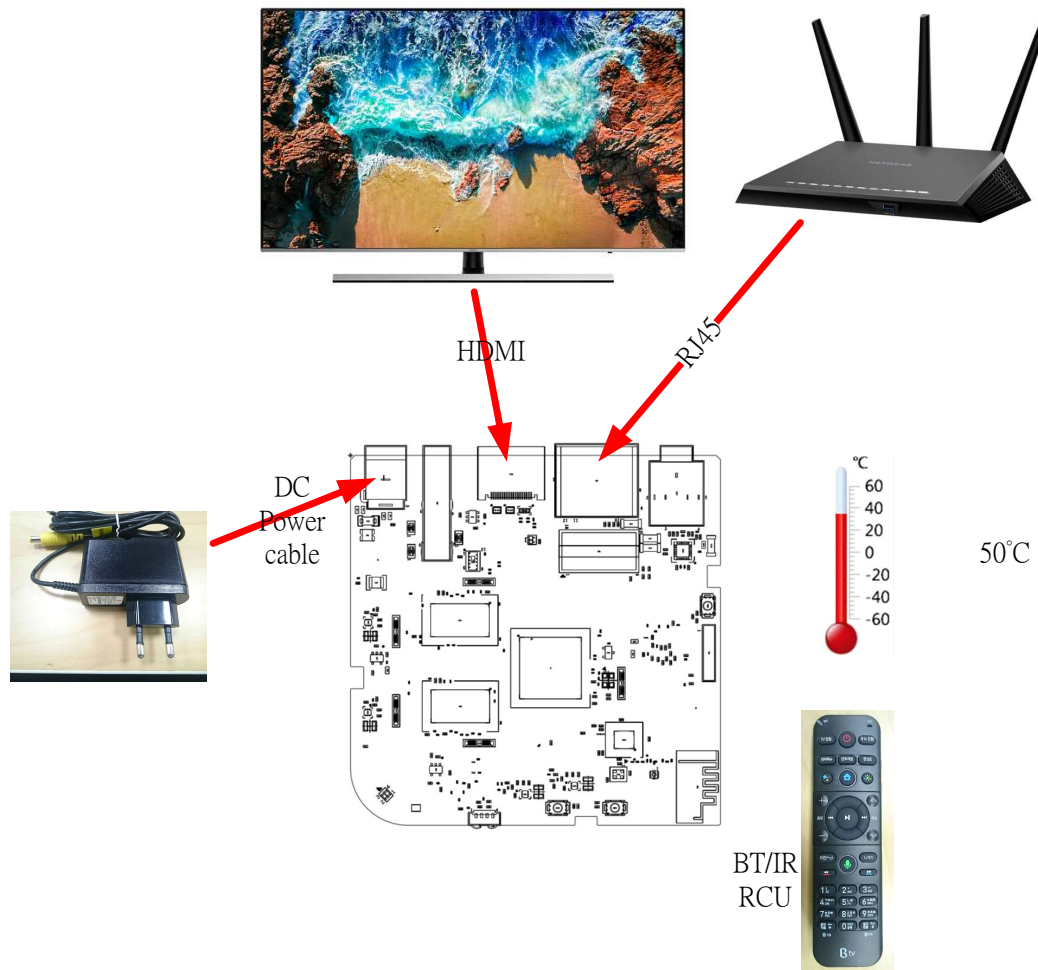


Fig. 11: PP_PWR_IN with USB 900mA load

3. Power Test Setup (3)



3.1 Test Condition

BOX play 4K video via Ethernet by using YouTube. HDMI output port connects to TV through HDMI cable. The temperature is about 50 degrees.

3.2 Result and Picture

Power Rail	Specification (V) (+5%)			Test Result (V)	Figure	Pass/Fail
	Min.	Typ.	Max.			
PP_PWR_IN (5V)	4.75	5	5.25	5.085	Figure 12	Pass
HDMI_PW (5V)	4.75	5	5.25	5.1	Figure 13	Pass
USB_5V (5V)	4.75	5	5.25	5.076	Figure 14	Pass
VDD_EE(0.8V)	0.77	0.8	0.9	0.8361	Figure 15	Pass
VDDCPU *	0.68	1	1.03	1.005	Figure 16	Pass
P3V3 (3.3V)	3.15	3.3	3.45	3.36	Figure 17	Pass
P2V5 (2.5V)	2.375	2.5	2.625	2.502	Figure 18	Pass
P1V8 (1.8V)	1.71	1.8	1.89	1.788	Figure 19	Pass
EMMC_VDDQ (1.8V)	1.71	1.8	1.89	1.805	Figure 20	Pass
P1V2 (1.2V)	1.14	1.2	1.26	1.192	Figure 21	Pass

Note * VDDCPU power rail is using voltage identification and control by PWM. This report is fix in 1V.

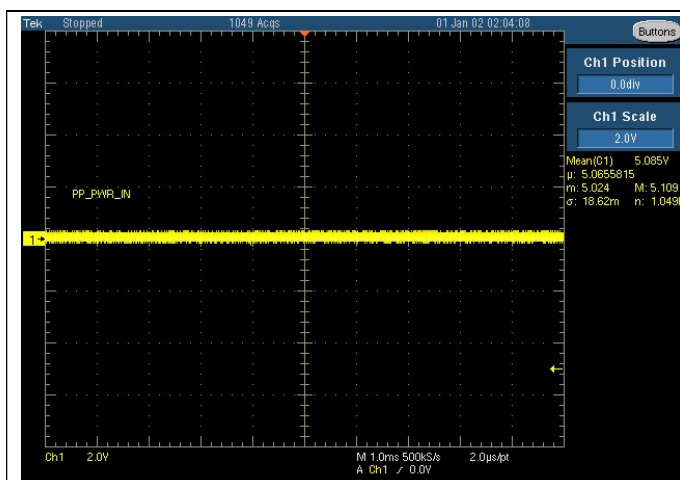


Fig. 12: PP_PWR_IN



Fig. 13: HDMI_PW



Fig. 14: USB_5V

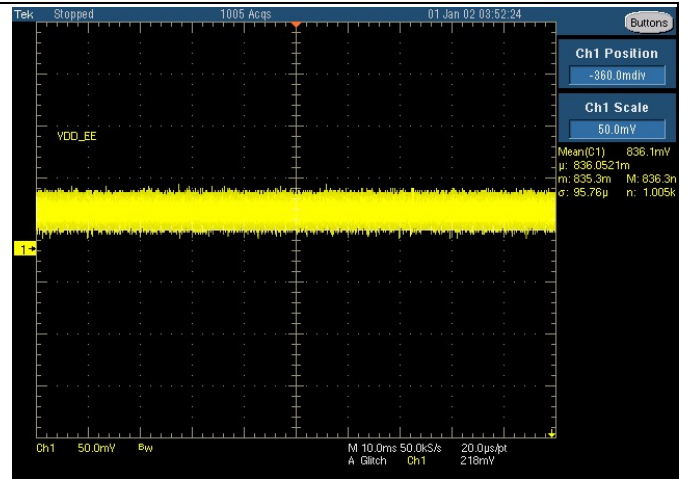


Fig. 15: VDD_EE

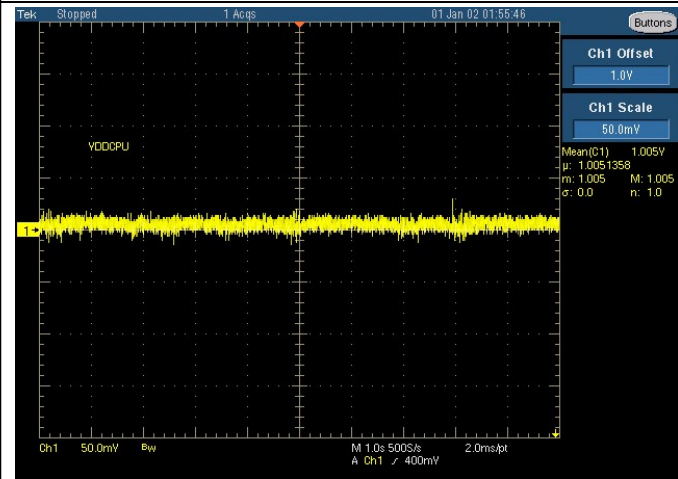


Fig. 16: VDDCPU

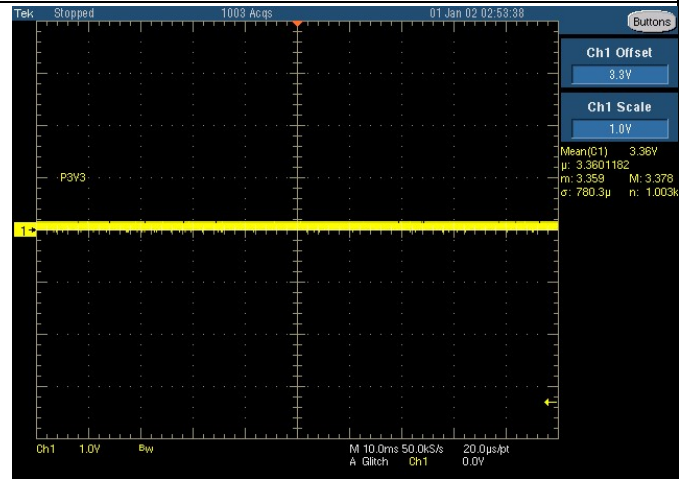


Fig. 17: P3V3

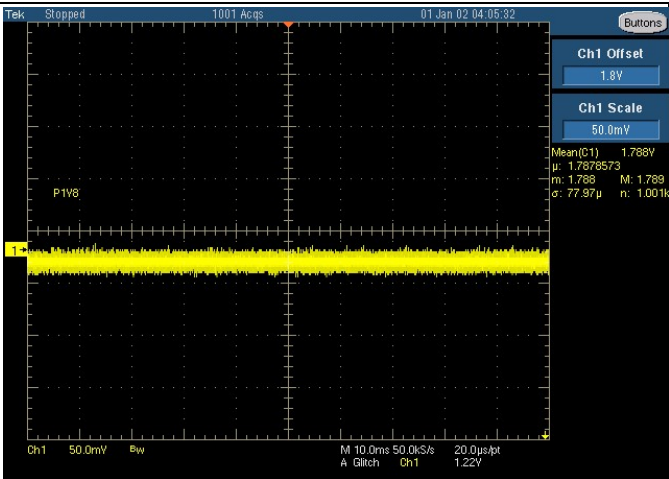
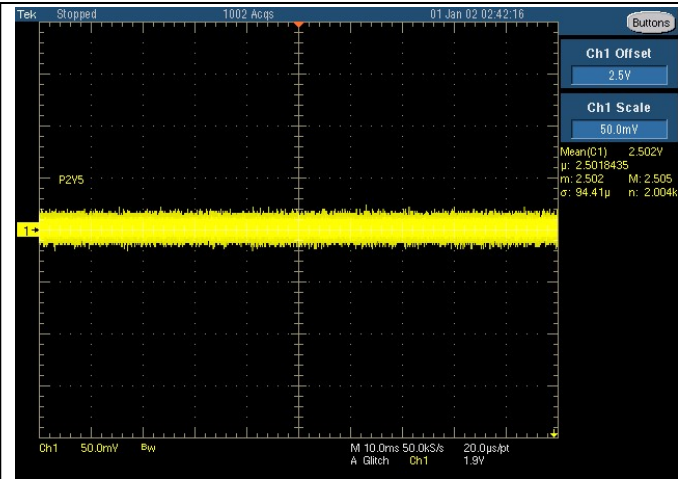


Fig. 18: P2V5

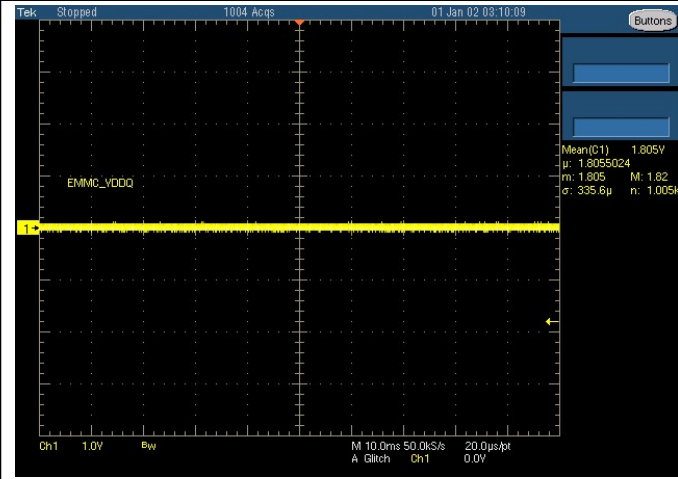


Fig. 20: EMMC_VDDQ

Fig. 19: P1V8

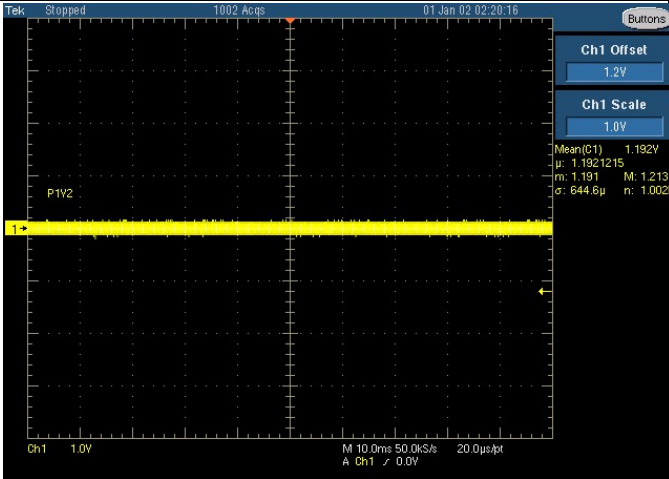
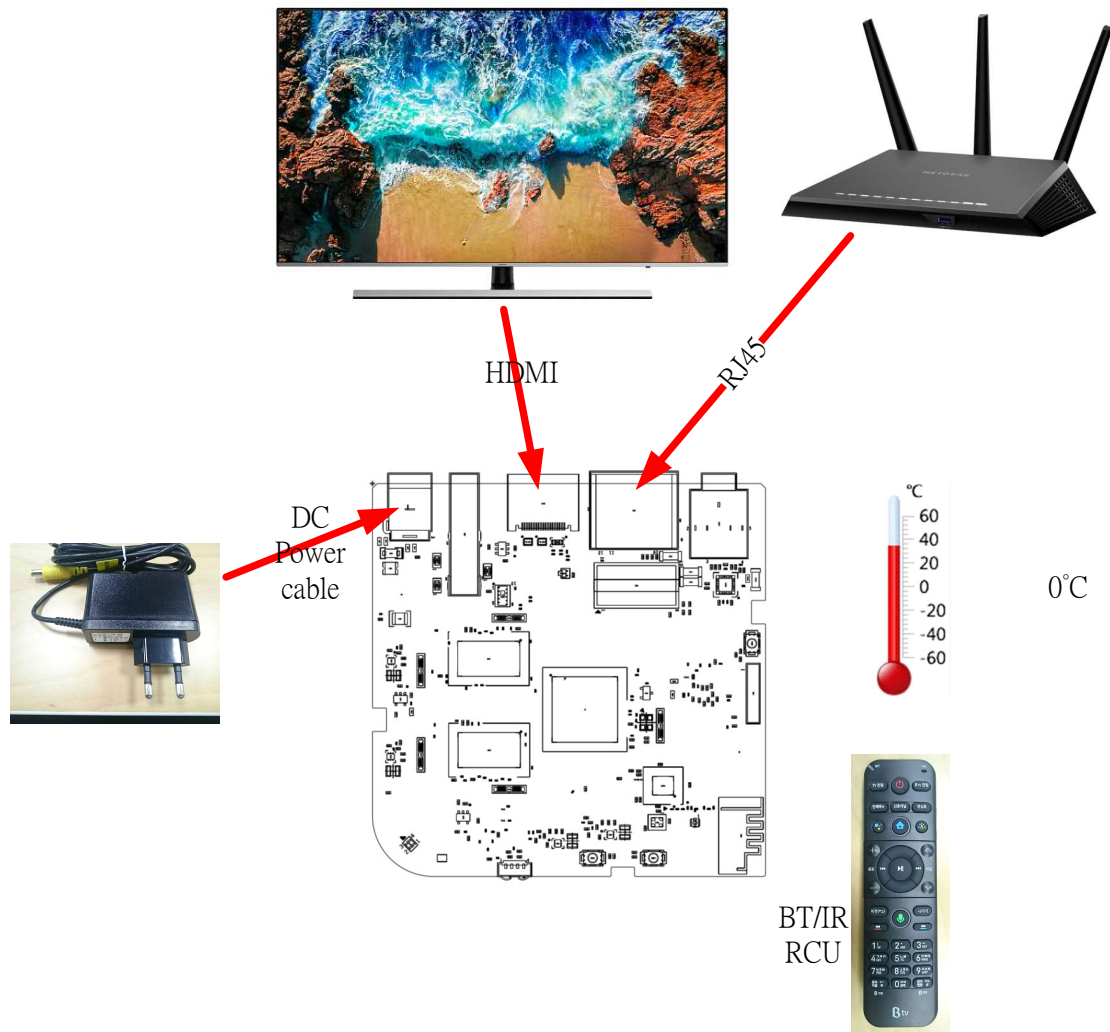


Fig. 21: P1V2

4. Power Test Setup (4)



4.1 Test Condition

BOX play 4K video via Ethernet by using YouTube. HDMI output port connects to TV through HDMI cable. The temperature is about 0 degrees.

4.2 Result and Picture

Power Rail	Specification (V) (+5%)			Test Result (V)	Figure	Pass/Fail
	Min.	Typ.	Max.			
PP_PWR_IN (5V)	4.75	5	5.25	5.11	Figure 22	Pass
HDMI_PW (5V)	4.75	5	5.25	5.095	Figure 23	Pass
USB_5V (5V)	4.75	5	5.25	5.06	Figure 24	Pass
VDD_EE(0.8V)	0.77	0.8	0.9	0.8381	Figure 25	Pass
VDDCPU	0.68	1	1.03	1.005	Figure 26	Pass
P3V3 (3.3V)	3.15	3.3	3.45	3.325	Figure 27	Pass
P2V5 (2.5V)	2.375	2.5	2.625	2.529	Figure 28	Pass
P1V8 (1.8V)	1.71	1.8	1.89	1.821	Figure 29	Pass
EMMC_VDDQ (1.8V)	1.71	1.8	1.89	1.83	Figure 30	Pass
P1V2 (1.2V)	1.14	1.2	1.26	1.227	Figure 31	Pass

Note * VDDCPU power rail is using voltage identification and control by PWM. This report is fix in 1V.

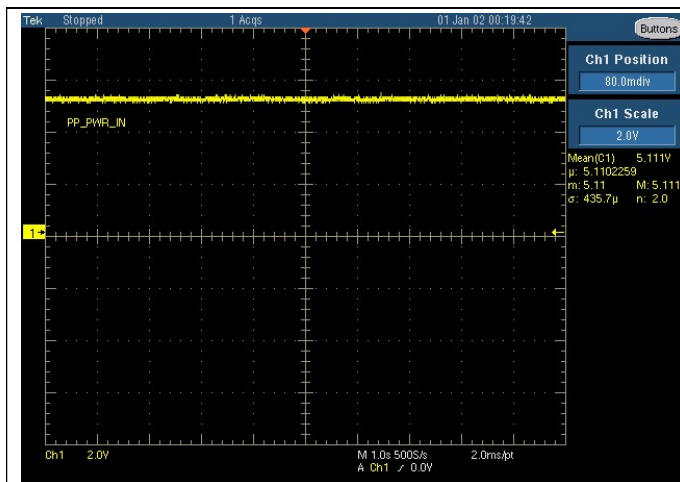


Fig. 22: PP_PWR_IN

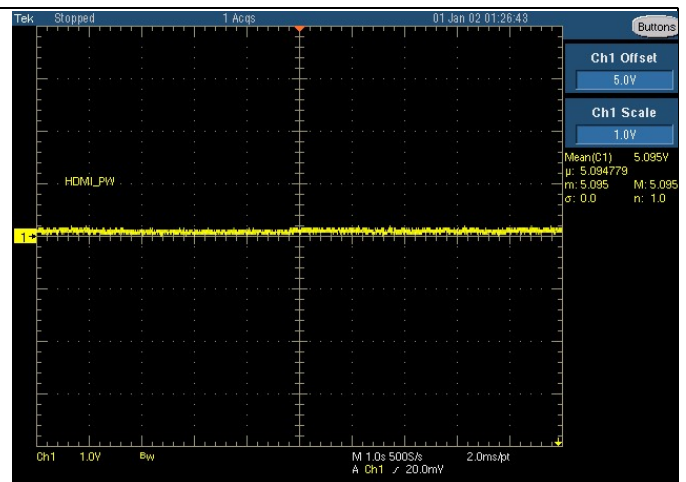


Fig. 23: HDMI_PW

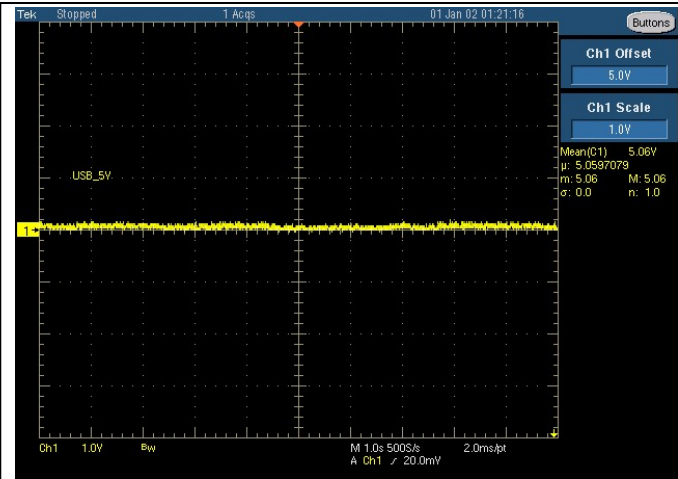


Fig. 24: USB_5V

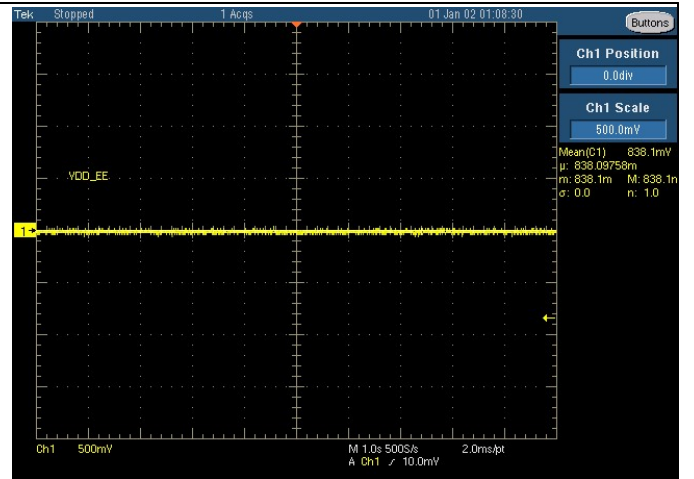


Fig. 25: VDD_EE

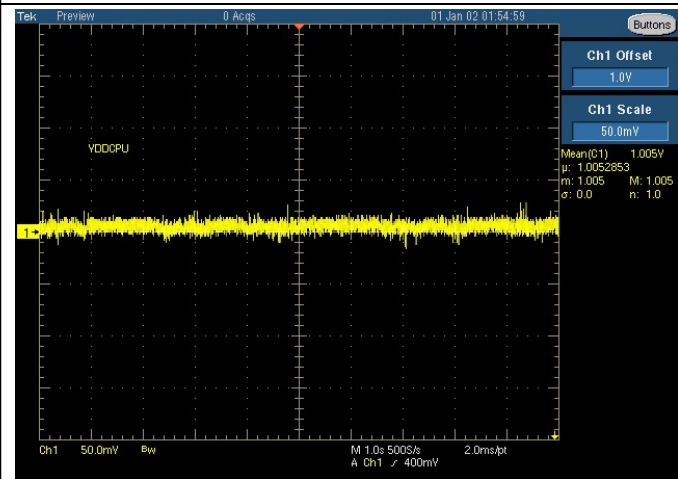


Fig. 26: VDDCPU

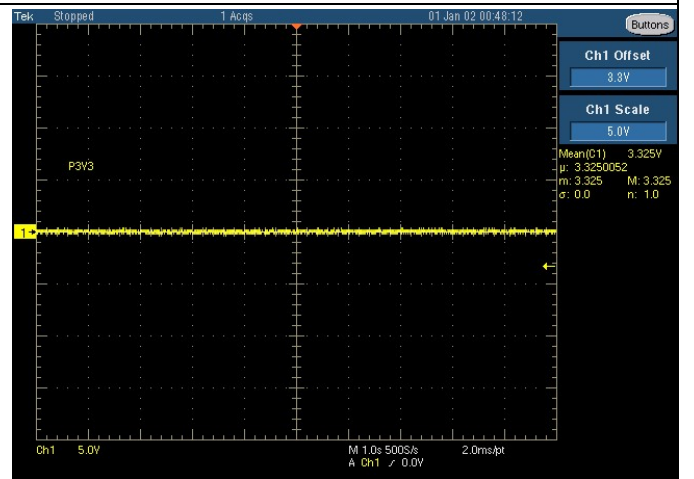


Fig. 27: P3V3

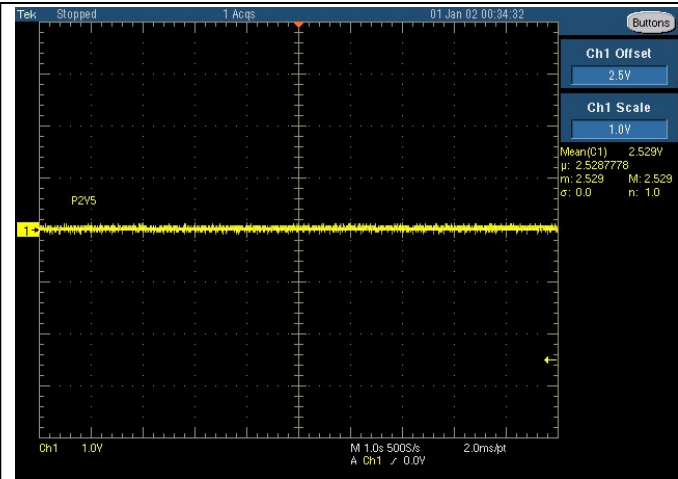


Fig. 28: P2V5

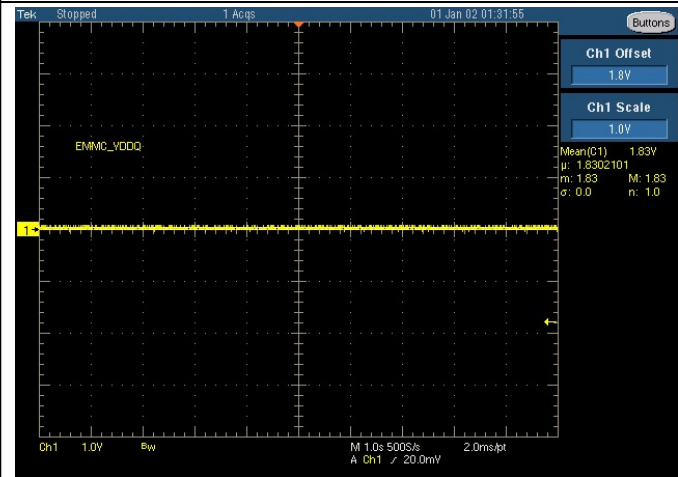


Fig. 30: EMMC_VDDQ

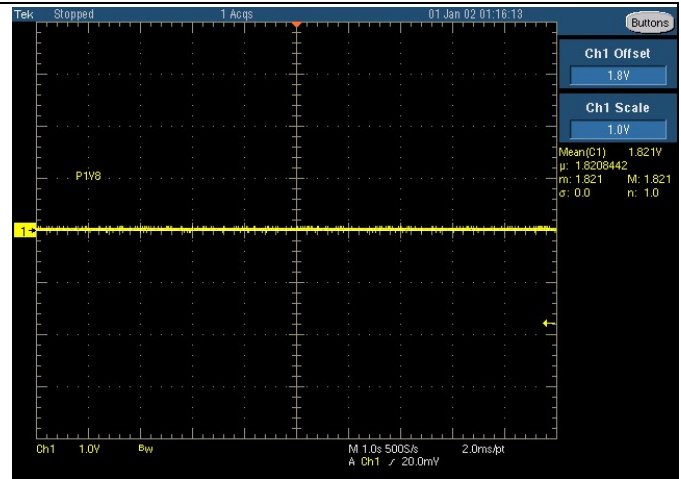


Fig. 29: P1V8

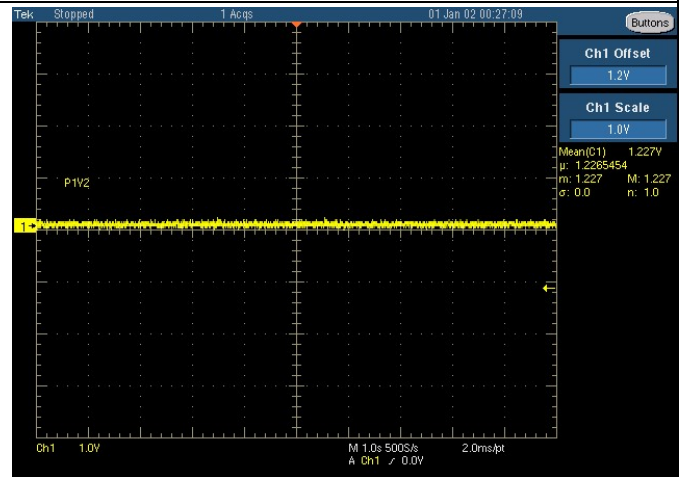


Fig. 31: P1V2